REMARKS

Prior to entry of this amendment, claims 1-12, 16-25, and 29-41 are pending. By this Amendment, non-elected claims 1-12, 16, 17, 22-25, 29, and 31-41 are canceled. Applicant reserves the right to file a divisional application on the non-elected claims at any point prior to the termination of the proceedings in the subject application.

Also by this Amendment, claims 18-21 are amended. No new matter is added. Claims 18-21 and 30 are presented for further prosecution on the merits.

Favorable reconsideration of this application is respectfully requested in view of the foregoing amendments and following remarks.

Claim Objection

In the Office Action mailed November 1, 2004, claim 20 was objected to because the Examiner was unable to find the language "a third wiring layer," "a second semiconductor substrate" and "a fourth wiring layer" in the specification.

It is respectfully submitted that the "third wiring layer," the "second semiconductor substrate" and the "fourth wiring layer" of claim 20 respectively correspond to the multi-level wiring layer 35, the substrate 33, and the large-size bus wiring layer 38A of the logic chip 10A illustrated in Fig. 15 and described in the specification as filed at p. 24, line 24 – p. 30, line 26.

As disclosed in the specification at p. 6, lines 11-18, Fig. 13 illustrates an embodiment of a multi-chip semiconductor apparatus of the claimed invention. Fig. 14 illustrates a cross section taken at a portion "I" of a memory chip (20A) of the multi-chip semiconductor apparatus of Fig. 13. Fig. 15 illustrates a cross

section taken at a portion "II" of a logic chip (10A) of the multi-chip semiconductor apparatus of Fig. 13. Thus, Figs. 14 and 15 illustrate portions of the memory chip of Fig. 13 and the logic chip of Fig. 13, respectively.

The specification further discloses at p. 26, lines 34-36, that in Fig. 15, the elements that are essentially the same as corresponding elements in Fig. 14 are designated by the same reference numerals, for the sake of simplicity of description. Therefore, the multi-level wiring layer 35, the substrate 33, and the large-size bus wiring layer 38 or 38A of the memory chip 20A and the logic chip 10A illustrated in Figs. 14 and 15, respectively, are called the same thing in the specification, but are described as being distinct and as being positioned on distinct chips, i.e., the memory chip 20A and the logic chip 10A of the multi-chip semiconductor apparatus. For clarity, in claim 20, these elements are claimed as being distinct. In particular, claim 20 recites, in part:

> A multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components...
> **the first chip comprising:**
> a **first** wiring layer provided on a **first** semiconductor substrate;
> a **second** wiring layer...
> **the second chip comprising:**
> a **third** wiring layer provided on a **second** semiconductor substrate;
> a **fourth** wiring layer...[Emphasis added]

It is respectfully submitted that claim 20 and the specification are in compliance with the rules of U.S. patent practice, and withdrawal of the objection is requested.

Claims 18-21 and 30 Recite Patentable Subject Matter

In the Office Action mailed November 1, 2004, claims 18-21 were rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 6,403,463 to Suyama (hereinafter, "Suyama"), and claim 30 was rejected under 35 USC § 103(a) as being unpatentable over Suyama in view of U.S. Patent Application Publication No. 2002/0004932 to Shau (hereinafter, "Shau").

It is noted that claims 18-21 have been amended. To the extent that the rejections apply to the claims currently pending, applicant hereby traverses the rejections, as follows.

Claims 18-21 are each directed to a multi-chip semiconductor apparatus in which a first chip and a second chip coexist. Each of claims 18-21 includes, among others, a feature wherein the first chip and the second chip are disposed so that the circuit surface of the first chip and the circuit surface of the second chip confront each other. By this configuration, the electrodes on the circuit components of the first chip and the electrodes on the circuit components of the second chip are easily interconnected by the conductive lines on one of the first and second chips. Further, the claimed configuration of the first and second chips provides for the use of shortened conductive lines, enabling operation of the chips at a low driving voltage with a small parasitic capacitance and low wiring resistance. Thus, high-speed operation and reduced power consumption may be realized.

In contrast, Suyama discloses a multi-chip semiconductor apparatus including a plurality of LSI chips which are arranged side by side on the same plane. A thin-film wiring layer is disposed to cover the entire substrate so that the circuit components are interconnected by the conductive lines of the wiring layer. Since the chips of Suyama are arranged side by side, unlike in the claimed invention, the total length of the conductive lines to interconnect the circuit components of the chips is required to be longer, raising the parasitic capacitance. Additionally, this side by side arrangement means that these two chips cannot confront each other as recited in the present claims.

For at least the reasons set forth above, Applicant submits that Suyama fails to disclose or suggest each and every element of the claimed invention. Specifically, Suyama fails to disclose or suggest disposing the first chip and the second chip so that the circuit surface of the first chip and the circuit surface of the second chip confront each other. Therefore, claims 18-21 are neither anticipated nor rendered obvious by Suyama, and withdrawal of the rejection is respectfully requested.

Regarding the rejection of claim 30 under 35 USC § 103(a), the Office Action asserts that Shau discloses a combination of logic circuit modules 102 and memory modules 103. However, Shau is not cited for nor does Shau cure the deficiencies of Suyama noted above. Accordingly, the combination of Suyama and Shau fails to disclose or suggest disposing the first chip and the second chip so that the circuit surface of the first chip and the circuit surface of

the second chip confront each other, as recited in claim 19, from which claim 30 depends. Since the combination of Shau and Suyama fails to disclose or suggest each and every feature of claim 30, it is respectfully submitted that claim 30 is neither anticipated nor rendered obvious by the combination of these two references.

Accordingly, reconsideration and withdrawal of the rejection of claim 30 are respectfully requested.

Conclusion

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding objection and rejections, allowance of claims 18-21 and 30, and the prompt issuance of a Notice of Allowability are respectfully solicited.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to Deposit Account No. 01-2300 referencing Attorney Docket No. **100353-00181**.

Respectfully submitted,

ARENT FOX, PLLC

Michele L. Connell
Registration No. 52,763

Customer No. 004372
1050 Connecticut Avenue, N.W., Suite 400
Washington, D.C. 20036-5339
Ph (202) 857-6104
Fax (202) 857-6395

CMM/MLC:grs